HiperLAN 5.4-GHz Low-Power CMOS Synchronous Oscillator

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***Abstract*—A 5.4-GHz 0.25-μm very-large-scale-integration CMOS synchronous oscillator (SO) is proposed in this paper, which is designed to act as a local oscillator for hiperLAN systems. The advantage of using such an oscillator in a double-loop frequency synthesizer is demonstrated. The design strategy leading to an optimized SO with regards to its synchronization range is described. A test chip is presented, which provides a 150-MHz synchronization range and a −97-dBc/Hz phase noise at 10-kHz offset from the 5-GHz carrier, while consuming only 5 mA from a 2.5-V supply.**

***Index Terms*—CMOS technology, frequency synthesizers, oscillators, phase-locked loops.**

I. Introduction

THE new hiperLAN standard defines, among others, a frequency band from 5.15 up to 5.25 GHz for future RF digital data transmission systems. While a 100-MHz-wide frequency band centered at roughly 5 GHz is not a stringent constraint, such a high frequency of interest will no doubt induce large power consumption within the frequency synthesizer. This will mostly be due to the frequency dividers. In addition, for the dividers to be able to handle 5-GHz signals, advanced technologies are mandated. Thus making both low-cost and low-power systems difficult, if not impossible, to achieve.

In addition to achieving low-power behavior, a hiperLAN system will also have to provide a frequency-agile synthesizer for the transceiver to deal with spread-spectrum multiple-access techniques. This will require a high-performance fractional synthesizer or multiple loop architectures. This leads to complex frequency-generation circuits and, therefore, a large silicon area, as well as excessive power consumption.

On the other hand, synchronous oscillator (SO)-based synthesizers had been previously proposed as an alternative to a phase-locked-loop (PLL)-based synthesizer [1], [2]. Indeed, the injection-locked phenomena SO takes advantage of leads to very compact PLL-like circuits. As no further frequency divider is needed in an SO, power consumption is also dramatically reduced with regards to its PLL counterparts, and classical technologies such as very-large-scale-integration (VLSI) CMOS can still be brought into play.

This paper presents a 5.4-GHz SO, which is implemented in such a VLSI CMOS technology. The circuit is designed to act as a local oscillator in a superheterodyne HiperLAN receiver with a 200-MHz intermediate frequency. First, the bandwidth advantage of a double-loop synthesizer is detailed, emphasizing an SO-based architecture. Based on an SO theory derived from [3], the design strategy leading to an optimized SO is then proposed. The chip is then described, and experimental results are then given, which highlight the excellent behavior of the circuit.

II. SO-Based Double-Loop Synthesizer Principle

The multiple-access technique retained for hiperLAN relies on the spectrum-spreading technique. It compels the synthesizer to bear as large a bandwidth as possible, which means that it has to offer the largest possible natural frequency [4], [5]. Thus, the synthesizer design appears to be very challenging, and a fractional architecture is required [5].

In addition to fractional synthesis, multiple-loop synthesizer can be implemented to further improve the overall bandwidth. Indeed, for a given technology, the association of both the phase frequency detector (PFD) and charge pump (CP) is able to deal with maximum frequency. We can denoted this maximum frequency as $F_{\max}$. Today, the latter is a few tens of megahertz. It leads to a frequency division ratio N of roughly 500 whenever a single-loop fractional PLL has to provide the hiperLAN 5-GHz local oscillator from a 10-MHz reference. For the most classical Type-2 second-order loop [4], the natural frequency ω_n is expressed as

$$\omega_n = \frac{\omega_{n1}}{\sqrt{N}} \tag{1}$$

where ω_{n1} is the loop natural frequency without any frequency division and N is the above-mentioned frequency division ratio. Hence, the single-loop synthesizer bandwidth, which is proportional to this natural frequency, is roughly 22 times smaller than that of a virtual "no frequency shift" PLL—i.e., a PLL without a divider in its feedback loop.

On the other hand, if the synthesizer is built with a double-loop architecture (the first low-frequency loop providing a frequency division of 42 and the second RF loop providing a frequency division of 12) while the overall frequency division ratio is still roughly 500, an increase of the bandwidth is obtained.

Indeed, let us suppose the low-frequency loop synthesizes 420 MHz from the still 10-MHz reference. Assuming the same

Manuscript received March 30, 2001. This work was supported in part by the European Community and by the French Government under the MicroElectronique Development for European Applications T555 ASGRA Project.

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Publisher Item Identifier S 0018-9480(01)07575-5.

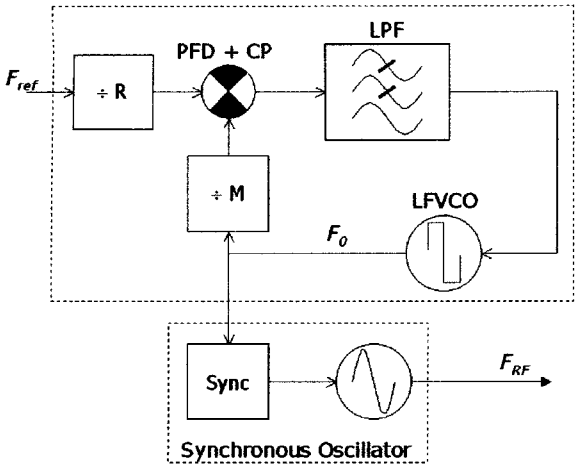

Fig. 1. SO-based double-loop frequency synthesizer principle.

ω_{n1} "no frequency shift" natural frequency, (1) highlights a natural frequency for the low-frequency loop roughly seven times smaller than ω_{n1}. If we still assume the same ω_{n1} for the RF frequency loop, the latter synthesizes the 5 GHz from the 420 MHz with a similar bandwidth since the natural frequency is not related to the synthesized frequency [4]. The overall synthesizer bandwidth is, therefore, roughly only seven times smaller than that of a virtual "no frequency shift" PLL and, consequently, three times larger than that of a single-loop synthesizer.

These presented values are only "rules of thumb" examples, and performing thorough computation can either lead to better or worst results. Though, it emphasizes the double-loop advantages when a careful attention is given to loop design.

Nonetheless, the previous first-order computation supposes that the high-frequency loop is able to deal with a 420-MHz reference, which is not compatible with what we said was $F_{\max}$. It is still possible—although difficult—to realize this kind of RF PLL if the loop does not have to deal with channel selection [6], leading to a fixed division ratio, and then to lesser stringent constraints for the loop. This approach obviously makes matters worse for the low-frequency loop, which is now solely responsible for the overall synthesizer channel selection. However, reporting the constraint on low-frequency electronics is not so bad a principle.

While such a complex a double-loop synthesizer will reach the hiperLAN requirements, it will also consume too high a current with regard to the behavior of the final application. On the other hand, one can take advantage of the SO to replace the high-frequency (RF) PLL in a double-loop synthesizer. Such an approach will result in a low-power and still quite simple synthesizer, while increasing wide bandwidth and high-speed performances.

The principle of the proposed synthesizer is depicted in Fig. 1.

In Fig. 1, we can see the low-frequency PLL with its low-frequency voltage-controlled oscillator (LFVCO). The intermediate frequency F_0 is related to the reference frequency $F_{\rm ref}$ as

$$F_0 = F_{\rm ref} \cdot \frac{M}{R}. \tag{2}$$

Assuming subharmonic synchronization [2], a major property of an SO, the RF output frequency is then expressed as

$$F_{\rm RF} = F_{\rm ref} \cdot \frac{M \cdot H}{R} = N \cdot F_{\rm ref} \tag{3}$$

where H is the subharmonic synchronization rank of the SO. The M divider might be a fractional one to increase the low-frequency PLL bandwidth, and the LFVCO might be a low-noise relaxation oscillator [7] to reduce the out-of-band phase noise of the overall synthesizer.

Hence, as previously mentioned, with a twelfth subharmonic synchronization scheme for the SO, the low-frequency loop will exhibit about 3.5 times larger a bandwidth than a single-loop counterpart.

While an SO is a PLL-like system, it is definitively not a PLL. Indeed, the SO will synchronize on the twelfth harmonic of the low-frequency PLL output, meaning that the first out-of-band parasitic signal of the low-frequency loop fundamental is 12 times away from its twelfth harmonic: the bandwidth is 12 times larger for the twelfth harmonic than it was for the fundamental. Assuming first-order calculation and that the SO have an infinite bandwidth—or at least a sufficient one—the overall synthesizer will, therefore, carry out a roughly 40 times larger bandwidth than that of a single-loop fractional synthesizer.

In addition, as the SO appears to be a very small and simple circuit, the overall SO-based double-loop frequency synthesizer has a low-power and low silicon-area behavior, which demonstrates the proposed SO-based double-loop synthesizer advantages, assuming that the SO has been optimized for its synchronization range to be as large as possible.

III. Design Strategy Leading to Optimized SO

A. Theoretical Synchronization Range

The theory proposed in [3] can be adapted to suit modern microelectronic circuits with only minor changes. It leads to the synchronization range of the SO, a property similar to the lock range of the PLL [4] as follows:

$$\Delta f = 2 \cdot \frac{|I_{\rm sync}|}{|V_{\rm osc}|} \cdot \sqrt{F_g^2 + F_b^2} \tag{4}$$

where Δf is the synchronization range, $I_{\rm sync}$ is the synchronization current, $V_{\rm osc}$ is the free-running oscillation amplitude, and F_g and F_b are the so-called "compliance factors," which are, respectively, the sensitivities of the oscillator frequency with regard to variations in the real and imaginary parts of the *LC* tank impedance.

B. Bandwidth Optimization

Thanks to the theory, an expression of the SO bandwidth (BW) is obtained as follows:

$$\mathrm{BW} = \frac{\Delta f}{2} \cdot \sin\left(\arccos\left(\frac{2(f_1 - f_0)}{\Delta f}\right)\right) \tag{5}$$

where Δf is the synchronization range, f_0 is the free-running oscillation frequency, and f_1 is the synchronization signal fre-

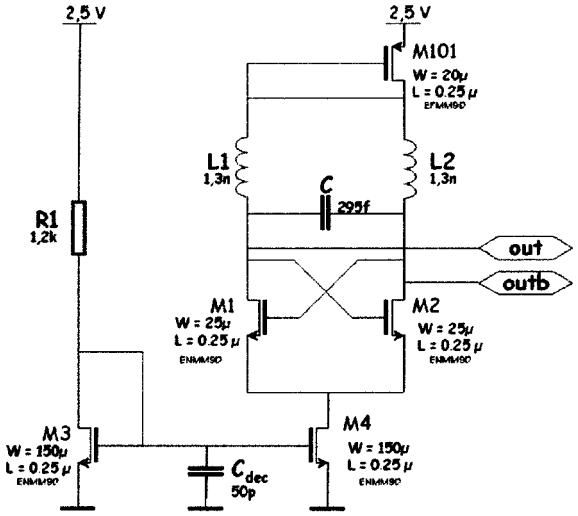

Fig. 2. Negative resistor oscillator.

quency. Within this bandwidth, the SO merely copies the synchronization signal phase noise. Due to stability reasons, the BW is always positive.

Unlike the PLL, (5) exposes that an SO bandwidth is strongly related to its locked frequency. However, with Δf classical values, the BW is always in the range of a few tens of megahertz. Such a characteristic is very difficult to obtain in PLL systems [4], even with fractional dividers [5].

As a matter of consequence, the larger the synchronization range, the lower the SO-based synthesizer phase noise can be. Equation (4) demonstrates that it can be obtained with both large compliance factors and large synchronization current.

C. Compliance Factor Optimization

A compliance factors computation for usual oscillator architectures establishes that, among these architectures, both Colpitts and "negative-resistor" topologies are providing the largest synchronization range. Nonetheless, the latter was preferred as the negative-resistor oscillator differential nature adds substrate coupling immunity for free.

The oscillator schematic is depicted in Fig. 2.

The first-order synchronization range for this circuit is then given by (6)

$$\Delta f = \frac{1}{2\pi} \cdot \frac{|I_{\text{sync}}|}{|V_{\text{osc}}|} \cdot \frac{1}{C} \tag{6}$$

with C being the overall tank capacitor, including the parasitic. A tradeoff between inductance parameters, power consumption, and self-resonance effects leads to the components values shown in Fig. 2. Its yields a 600-mV differential free-running oscillation amplitude, and a roughly 5.4-GHz free-running frequency.

D. Synchronization Current Optimization

We are looking for a subharmonic synchronization process [1] with a 450-MHz synchronization signal to lock the SO at 5.4 GHz, i.e., the twelfth harmonic. Hence, the synchronization current waveform has been chosen as depicted in Fig. 3.

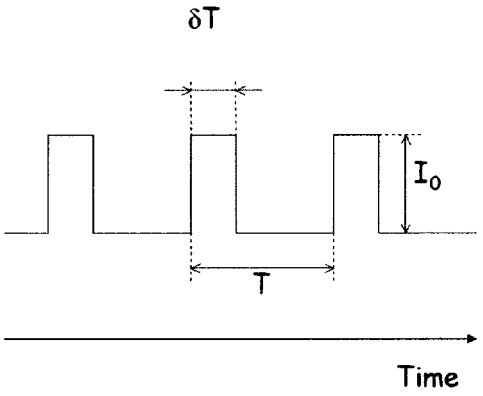

Fig. 3. Synchronization current waveform.

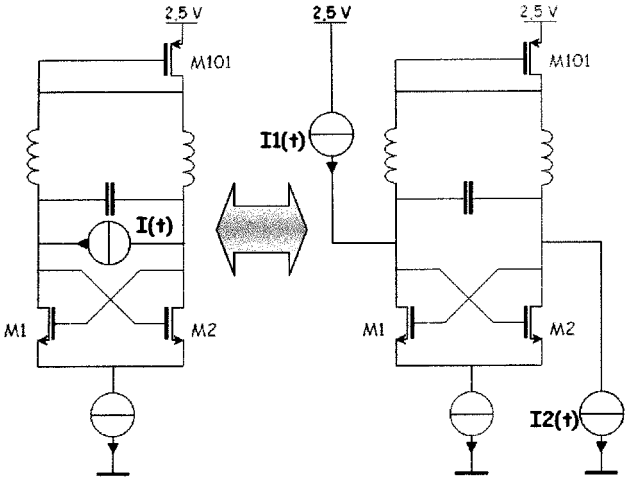

Fig. 4. "Floating" current realization.

Such a waveform has an nth harmonic amplitude of

$$I_n = \frac{I_0\sqrt{2}}{n\pi} \cdot \sqrt{1-\cos(2n\delta\pi)}. \tag{7}$$

A maximum is obtained when the pulse duration is exactly 50% of the SO output signal period. With the components values of Fig. 2, a 400-μA twelfth harmonic current amplitude is needed to provide a 150-MHz frequency range, which is well suited for our HiperLAN application—including a margin. It imposes a 4-mA current pulse at the wanted 450-MHz synchronization signal frequency.

Fig. 4 emphasizes the way we design the "floating" current synchronization source $I(t)$ with two asymmetric current sources $I_1(t)$ and $I_2(t)$. While this approach reduces the differential advantage, it is far easier to implement. It is the reason why M_{101} was added in the negative resistor oscillator, as it provides voltage headroom for the $I_1(t)$ PMOS current switch.

Fig. 5 depicted the current pulse generator, based on a delay-oriented design (DOD) approach [6].

E. Overall SO

Both the NAND and inverters MOSFET dimensions in Fig. 5 were carefully chosen so as to provide a 4-mA output current pulse duration of around 100 ps, which is in good agreement

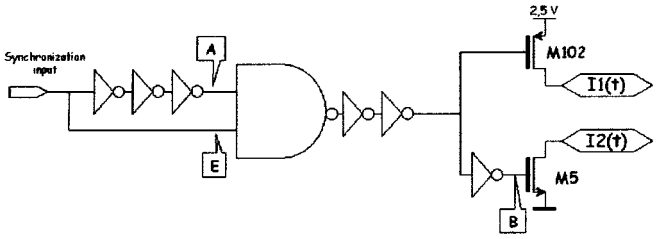

Fig. 5. Current pulse generator.

with the optimum value given by (7). It yields a twelfth harmonic current amplitude of 420 μA, leading to a theoretical synchronization range of 160 MHz, according to the above-mentioned 600-mV differential free-running oscillation amplitude.

In these conditions, the overall SO—i.e., the negative resistor oscillator of Fig. 1 and the current pulse generator of Fig. 4—sinks 3 mA from the 2.5-V voltage supply. According to (5), the bandwidth of this SO in the hiperLAN frequency range is always larger than 50 MHz. Hence, though the SO is a PLL-like system, its characteristics largely outclass those of a real PLL.

IV. 0.25-μm CMOS Chip

An HCMOS7 technology chip was manufactured by STMicroelectronics, Crolles, France, i.e., a 0.25-μm CMOS technology with six interconnection layers.

The hollow spiral inductors were designed with the last two metal layers in parallel, leading to a quality factor of roughly five due to the low-resistivity CMOS substrate.

The *LC* tank capacitor quality factor is as important as the inductor one. To avoid both the low quality factor associated with polysilicon capacitors as well as non-VLSI and, thus, expensive technology steps, the tuning capacitor was designed as a pseudofractal lateral flux capacitor [1], [8]. Practically speaking, two series capacitors were used to help maintaining the differential nature of the negative resistor oscillator.

Fig. 6 depicts the chip microphotograph. One can see both of the two hollow spiral inductors and the two lateral flux capacitors. Most of the remaining circuit parts are covered by dummy metals, which are mandated to preserve chip planarization.

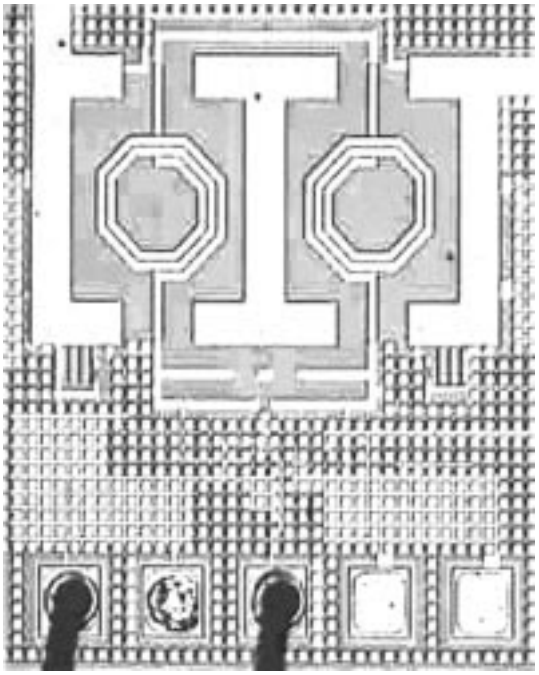

Fig. 6. Chip microphotograph.

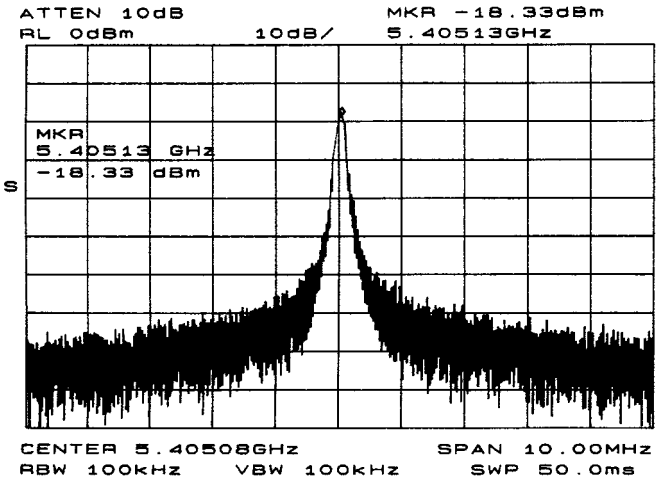

Fig. 7. Free-running spectrum.

V. Experimental Results

The chip was encapsulated in a TQFP32 classical plastic package, and soldered on a specific printed circuit board (PCB) in low-cost FR2 epoxy. Measurements were then performed with an HP8563E spectrum analyzer, and with an HP8648 signal generator whenever synchronization was needed. Indeed, the generator provides a sinusoidal signal of around 450 MHz, which acts as the synchronization signal for the SO to synchronize on the twelfth harmonic, at roughly 5.4 GHz. The dc voltage bias is 2.5 V.

A. Free-Running Oscillator

In the free-running mode, a dc current consumption of 42 mA was measured. The two 50-Ω buffers included within the chip are the major culprit, as they are expected from simulation to sink more or less 20 mA each. It yields a current consumption of 2–3 mA for the oscillator, which is in good agreement with simulations.

The free-running frequency is measured at 5.405 GHz, and the spectrum is depicted in Fig. 7.

The single-sideband (SSB) phase noise is depicted in Fig. 8. The low-offset plateau, i.e., for offset frequencies lower than 10 kHz, is due to the unlocked condition of measurement, and should not been taken into account.

While this phase noise should have little influence according to the 50 MHz of expected bandwidth, one can observe a -99-dBc/Hz spot at a 600-kHz offset from the carrier. This is not so bad a value with regard to the low-power-consumption behavior.

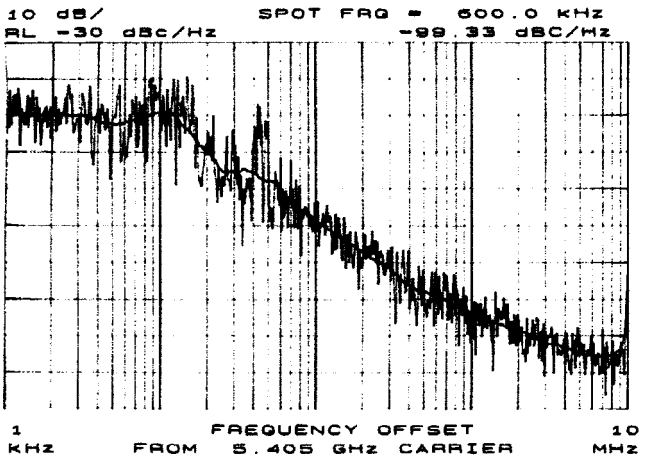

Fig. 8. Free-running SSB phase noise.

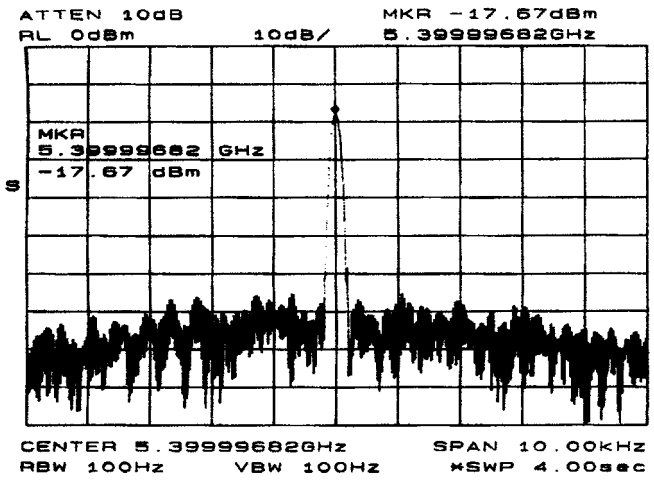

Fig. 9. Synchronized spectrum.

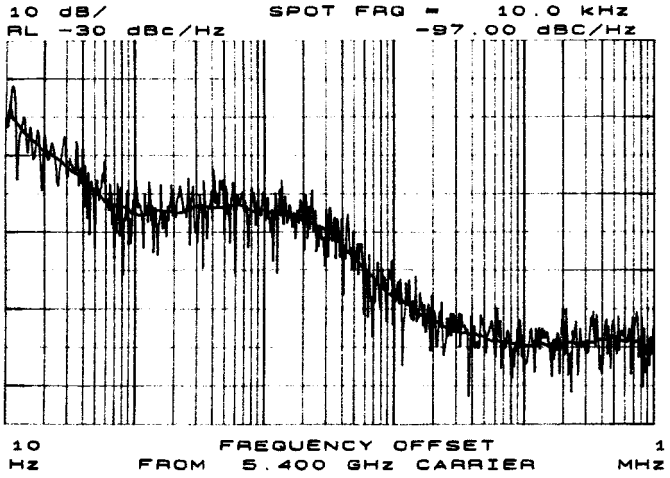

Fig. 10. Synchronized SSB phase noise.

TABLE I
SUMMARY OF SO CHARACTERISTICS

Quantity	Measured value
Technology	0.25 µm VLSI CMOS
Supply voltage	2.5 V
Output center frequency	5.4 GHz
Free running phase noise	-99 dBc/Hz @ 600 kHz
Input frequency	444 MHz to 456 MHz
Synchronization range	5.325 GHz to 5.475 GHz
SO current - synchronized	5 mA
Synchronized phase noise	-97 dBc/Hz @ 10 kHz (depending on reference)

B. Synchronized Oscillator

While synchronization is brought into play, a 2-mA increase in the dc current consumption is observed. This is due to the synchronization network, which is no longer idle.

A 450-MHz input signal leads to the 5.4–GHz SO output signal, of which the spectrum is illustrated in Fig. 9.

The 1-kHz per division at 5.4-GHz horizontal scale of Fig. 9 highlights the excellent stability of the SO in terms of frequency. The SSB phase noise depicted in Fig. 10 is a mere corroboration of this attribute. Indeed, a −97-dBc/Hz spot at 10-kHz offset of the carrier is obtained, i.e., a significant value for a full VLSI and low-power CMOS circuit.

The measured synchronization range coarsely spread from 444 up to 456 MHz for the input synchronization signal, corresponding to a 5.325- up to 5.475-GHz SO output signal. Thus, a 150-MHz range is observed, while a 160-MHz range was expected, leading to a 7% error. Taking into account the passive components dispersion, it is in good agreement with simulation results, and it stays HiperLAN compatible.

C. Phase-Noise Consideration—Limitations

As a matter of fact, the phase noise of the synchronization signal is mostly significant in the SO phase-noise performance. Indeed, as a classical PLL does, the SO phase noise is a bare copy of the synchronization signal one, shifted by the log conversion of the frequency-division ratio.

Hence, whenever a noisy synchronization signal is used, a high SO phase noise can be observed. Nevertheless, since it is obviously easier to obtain a low phase-noise signal at low frequency than in the RF frequency range, as some compensation techniques can be implemented, the combination of both a low-frequency low-phase noise reference and this SO yields to a low-power, low-phase noise, and low-cost frequency synthesizer.

VI. CONCLUSION

A 5.4-GHz full VLSI 0.25-μm CMOS SO has been presented in this paper. This SO is well suited to fulfill a low-power frequency synthesizer able to deal with HiperLAN requirements. The major measured characteristics of the chip are summarized in Table I.

Thanks to the very wide bandwidth of the SO, the oscillator performances are no longer of any interest, at least as long as it is still able to oscillate. Thus, a dramatic reduction in current consumption can be achieved, as the oscillator phase-noise op-

timization is not mandated anymore. In addition, VLSI CMOS technologies appear efficient, paving the way for low-cost RF systems that are required to sustain, as well as to strengthen, the present wireless revolution.

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